DESIGN AUTOMATION CONFERENCE 56
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XILINX

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assuring IC integrity

Advances in Formal Connectivity Checking
A Case Study on a Multi-Billion-Gate SoC

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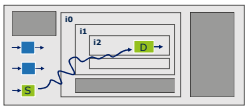
AI, 5G, Automotive Systems Require Huge SoCs

Connectivity verification ensures that blocks are integrated correctly



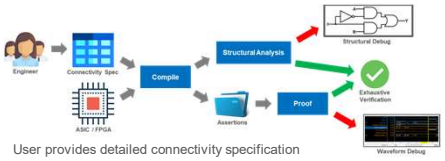
Connectivity bugs waste much effort
Often bugs are in the specification
Missing an issue could kill the chip

Challenges
- Bus wiring through many layers of hierarchy
- Highly configurable I/O pads
- Many IPs and other blocks
- Routing of global signals (clock, reset, debug, scan)
- Automated detection of delays
- … and more

1

Traditional Formal Connectivity Checking Flow

Exhaustive verification, sweet spot for formal
But does it scale?



User provides detailed connectivity specification
Assertions generation and exhaustive formal proof
Additional structural analysis needed to ensure physical connection

2

Traditional Connectivity Specification

High effort, hard to maintain, error prone

```
# Source            # Destination      # Delay # Condition          # clock
top.a.b.c,          top.x.y.z
top.i1_m_s_bit.x,   top.i1_m_d_bit.y, 1,      top.debug_en==1'b0, top.clk
top.i2_m_s_bit.x,   top.i2_m_d_bit.y, 2:3,    top.debug_en==1'b0, top.clk
top.i1_m_s_bot.x,   top.i1_m_d_bot.y, 5,      top.debug_en==1'b0, top.clk
top.i2_m_s_bot.x,   top.i2_m_d_bot.y, 2,      top.debug_en==1'b0, top.clk
```

One entry per connection - Must specify all details

3

Xilinx's Project Challenge

Traditional formal connectivity checking did not scale

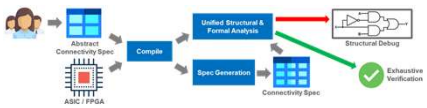
- Multi-billion gate SoC
- 7nm technology
- 35K modules
- 90M instances
- 170M flops
- 80K FSMs
- In excess of 1 million connections to specify, maintain across design iterations, and verify
- Tight design schedule
- No compromise on quality
- Exhaustive verification is crucial

Traditional connectivity checking apps **unsuccessful**
- **Excessive** runtime, **inconclusive** proof results
- Too much **effort** to create and maintain 1 million+ connections

4

Connectivity XL Flow

Innovative connectivity checking flow



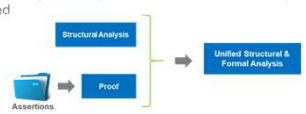
New approach to connectivity specification
New approach to connectivity checking proof algorithms

5

Connectivity XL Unified Proof

Merge structural and logical checks in one step

- Advanced, automated abstractions
- Proof localization: use the right proof engine on minimal required logic
- Stop/avoid logical analysis as soon as a connectivity issue is identified



6

Connectivity XL Abstract Specification

Connectivity XL generates the detailed connectivity specification

User provides the **abstract** connectivity specification

Connectivity XL may **expand** this into thousands of entries with delays, inverters, and multiplexing conditions **automatically**

7

Connectivity XL Abstract Specification Example

```
# Source                  # Destination
i:top.a.b, sig_c,         m:m_x,      sig_y
m:m_a,     sig_b,         i:top.x,    sig_y
m:m_s_b?p, sig_a,         m:m_d_b?p,  sig_x
m:m_s_b?t, sig_b,         m:m_d_b?t,  sig_y
m:m_s_b?o, sig_c,         m:m_d_b?o,  sig_z
m:m_s_*t,  sig_d,         m:m_d_*t,   sig_x
```

Source and destination can be module or instance signals
May use wildcards in names
May omit delays, change of polarity, multiplexing conditions
Customize leveraging coding guidelines and other rules

8

Results for Xilinx Project

High quality, exhaustive verification

Detected several corner-case bugs
- Incorrect block integration
- Multiple drivers and re-convergent paths
- Easy to root-cause issues, even for paths with more than 2K signals

Minimized risk of missing bugs
- 1M+ connections proven within days (using parallel jobs)
- No inconclusive proof results

9

Learnings

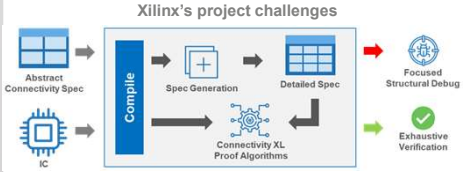
Abstract specifications are much simpler to handle

Reduced effort, avoided many human errors
- > **100x** compression factor using abstract specification
- Automated conditional connectivity checks (e.g., scan_en, debug_en)
- Automated identification of delay flops and inverters in connectivity path
- Elaborate design once, run connectivity checks multiple times

10

Summary

Connectivity XL successfully addressed Xilinx's project challenges



Automatic generation of detailed connectivity specification
Automatic proof localization for XL speed and capacity
Proven in 7nm, multi-billion-gate IC, 1M+ complex connections

11

Thank you!

Questions?

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12